This listing of claims will replace all prior versions and listings of claims in the application:

Listing of Claims:

1. (Currently amended) A method for processing a semiconductor topography, comprising:

polishing an upper layer of the semiconductor topography to expose a first underlying layer;

etching away remaining portions of said first underlying layer to expose a second underlying layer, wherein the first underlying layer is formed upon and in contact with the second underlying layer; and

subsequently planarizing the topography, wherein said planarizing comprises polishing the second underlying layer.

2. (Currently amended) The method of claim 1, wherein said polishing the upper layer comprises removing portions of the upper layer arranged above ~~the~~ an upper surface of the first underlying layer.

3. (Currently amended) The method of claim 1, wherein said polishing the upper layer ~~of the topography~~ comprises polishing a portion of the first underlying layer.

4. (Original) The method of claim 3, wherein a thickness of the first underlying layer is sufficient to prevent polishing through the first underlying layer during said polishing the upper layer.

5. (Currently amended) The method of claim 1, further comprising forming the upper layer, the first underlying layer, and the second underlying layer upon a semiconductor layer and in a single process chamber.

6. (Original) The method of claim 1, further comprising depositing the upper layer within a trench of the semiconductor topography prior to said polishing.

7. (Original) The method of claim 6, wherein said polishing the upper layer comprises polishing the upper layer such that remaining portions of the upper layer are laterally confined by sidewalls of the trench.

8. (Original) The method of claim 1, further comprising etching the planarized topography such that a third underlying layer is removed, wherein the third underlying layer is arranged beneath the second underlying layer.

9. (Currently amended) The method of claim 8, wherein said etching the planarized topography comprises removing a portion of the second underlying layer.

10. (Currently amended) A method for fabricating shallow trench isolation regions, comprising:

forming one or more trenches extending through a stack of at least three layers arranged over a semiconductor substrate, wherein the stack comprises intervening layers of different etching characteristics;

blanket depositing a dielectric over the one or more trenches and the stack ~~of layers~~ such that the one or more trenches are filled by the dielectric; and

planarizing the dielectric such that upper surfaces of the dielectric remaining within the one or more trenches are coplanar with an upper surface of an adjacent layer of the stack, wherein said planarizing comprises removing one or more of the at least three layers of the stack, and wherein said planarizing further comprises:

polishing the dielectric to expose an upper layer of the stack;

etching the upper layer to expose an intermediate layer of the stack, wherein the upper layer is formed upon and in contact with the intermediate layer; and

subsequently polishing the dielectric and the intermediate layer to expose the upper surface of the adjacent layer of the stack.

11. (Canceled)

12. (Currently amended) The method of claim ~~11~~10, wherein said subsequently polishing ~~the topography~~ is sufficient to produce a substantially planar surface without dishing portions of the adjacent layer.

13. (Currently amended) The method of claim ~~11~~10, wherein a thickness of said upper layer is between approximately 500 angstroms and approximately 1000 angstroms prior to said planarizing.

14. (Currently amended) The method of claim ~~11~~10, wherein said upper layer comprises silicon nitride.

15. (Currently amended) The method of claim ~~11~~10, wherein a thickness of said intermediate layer is between approximately 300 angstroms and approximately 700 angstroms prior to said planarizing.

16. (Currently amended) The method of claim ~~11~~10, wherein said intermediate layer comprises silicon dioxide.

17. (Currently amended) The method of claim ~~11~~10, wherein said intermediate layer and said dielectric comprise similar etch characteristics.

18. (Currently amended) The method of claim ~~11~~10, wherein said adjacent layer comprises the intermediate layer.

19. (Currently amended) The method of claim ~~11~~10, wherein said adjacent layer comprises a lower layer of the stack.

20. (Original) The method of claim 19, wherein a thickness of said lower layer is between approximately 300 angstroms and approximately 500 angstroms prior to said planarizing.

21. (Original) The method of claim 19, wherein said lower layer comprises silicon nitride.

22. (Original) The method of claim 10, further comprising etching the upper surface of the adjacent layer to expose the semiconductor substrate.

23. (Currently amended) The method of claim 22, wherein upper portions of the dielectric extend less than approximately 500 angstroms above ~~the~~ an upper surface of the semiconductor substrate subsequent to said etching the upper surface.

24. (Original) The method of claim 23, wherein the upper portions of the dielectric extend between approximately 300 angstroms and approximately 500 angstroms above the upper surface of the semiconductor substrate subsequent to said etching the upper surface.

25. (Currently amended) The method of claim 22, wherein average thicknesses of upper portions of the dielectric ~~layer~~ extending above the semiconductor substrate and corresponding to each of the one or more trenches differ by less than approximately 10%.